

**ABSTRACT OF THE DISCLOSURE**

A semiconductor integrated circuit having an embedded array wherein basic cells are arranged in a matrix is designed and manufactured (S1); a test is performed on whether an electrical behavior of a prototype of a semiconductor integrated circuit meets required specifications (S2); if meets, a non-use-area pattern in an embedded array area is detected and removed based on layout data of contact holes to get modified pattern (S4); a mask with a modified pattern is prepared (S5); and the mask is substituted for the mask before modification, thereby manufacturing a semiconductor integrated circuits from which a non-use area is removed (S6).

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